



**SANT LONGOWAL INSTITUTE OF ENGINEERING & TECHNOLOGY,  
LONGOWAL, SANGRUR – 148106 (Punjab)  
(Deemed to be University)  
(Under MoE-Govt. of India)**

**Ref No.: C2S/ECE/199**

**Date: 16-05-2024**

**ADVERTISEMENT**

Applications are invited for the one post of Project Associate-I in ECE Department, SLIET, Longowal under the research project sanction under Chips to Startup (C2S) scheme funded by Ministry of Electronics and Information Technology (MeitY), New Delhi, Government of India. The detailed Information is as per below:

| <b>Sr. No.</b> | <b>Head</b>                     | <b>Description</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1              | <b>Project Title</b>            | Design and Development of System-on-Chip for Single-Lead Wearable Electrocardiogram (ECG) for Medical Devices                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 2              | <b>Sponsoring Agency</b>        | Ministry of Electronics and Information Technology (MeitY), New Delhi, Government of India                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 3              | <b>Temporary Position</b>       | Project Associate-I : 01                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 4              | <b>Fellowship</b>               | <b>i.</b> Rs. 31,000/- per month to the candidate who is selected through (a) National Eligibility Tests <i>i.e.</i> CSIR/UGC/CBSE NET including Lectureship/Assistant Professorship or GATE.<br><b>ii.</b> Rs. 25000/- per month, for other who do not fall under <b>i.</b> above.                                                                                                                                                                                                                                                        |
| 5              | <b>Project Investigator</b>     | <b>Chief Investigator:</b> Dr. J S Ubhi, Professor, ECE<br><b>Co-Chief Investigator:</b> Dr. Surinder Singh, Professor, ECE.                                                                                                                                                                                                                                                                                                                                                                                                               |
| 6              | <b>Department</b>               | Department of Electronics and Communication Engineering                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 7              | <b>Tenure of the Assignment</b> | Initially for 06 months (subjected to be extended up to completion of project based on the performance)                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 8              | <b>Qualification</b>            | - Bachelor's degree in Engineering/Technology in Electronics and Communication or Electrical and Electronics Engineering or other relevant discipline with a minimum of 60% aggregate marks (or) CGPA of 6.5/10 in UG or PG for OC/OBC category candidates and 55% aggregate marks or equivalent CGPA of 6.0 for SC/ST candidates.                                                                                                                                                                                                         |
|                | <b>Desirable</b>                | - Candidates having Master's degree in Engineering/Technology in the fields of Electronics and Communication/ VLSI Design/ or related discipline with good academic record with GATE score will be preferable.<br>- Knowledge of Microelectronics and VLSI CAD tools (Cadence Virtuoso, Mentor Graphics, Synopsys, Siemens EDA Tools/TCAD/Xilinx), Analog IC Design, MATLAB.<br>- Knowledge of networking/ Linux-based operating system and relevant areas .<br>- <b>Preference will be given to candidates willing to enrol for Ph.D.</b> |
| 9              | <b>Age Limit</b>                | 35 years (5 years' relaxation for SC/ST/OBC/ female/Physically Handicapped Candidate).                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

Interested candidates may send their application with complete bio-data and photocopies of certificates by Email to Prof. J S Ubhi, Chief Investigator, Department of Electronics and Communication Engineering, Sant Longowal Institute of Engineering and Technology, Longowal, Sangrur-148106. (E-mail: [js\\_ubhi@yahoo.com](mailto:js_ubhi@yahoo.com)) on or before **30-05-2024**. The shortlisted candidates will be informed by mail/telephone. Selection will be based on qualification, interview (**OFFLINE**), research work & work experience in proposed field. No TA/DA will be paid for attending the interview (**OFFLINE**). SLIET Longowal reserves the right to reject any or all the applications without assigning any reasons thereof.

**Dr. Jagpal Singh Ubhi**  
**Chief Investigator, C2S Project**  
**& Professor (ECE Department), SLIET Longowal**  
**(M)-9463068009**

**Note:**

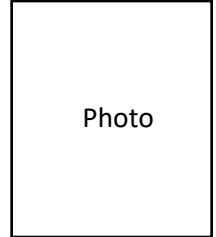
- Candidates before appearing for the selection process shall ensure that they are eligible for the position they intend to apply.
- Candidates applying for the Project Associate-I positions shall apply only through the email [js\\_ubhi@yahoo.com](mailto:js_ubhi@yahoo.com) on or before **30-05-2024**.
- The post will be tenable initially for a period of one year. It may be extended further at the discretion of duly constituted committee of SLIET, Longowal.
- The shortlisted candidates will be intimated about the selection process through e-mail.
- Candidates shall bring along with them the original certificates at the time of the selection process for verification.
- No TA/DA is admissible for attending the selection process.
- The decision of the selection committee is final. Canvassing in any form leads to the rejection of the candidature.
- The tenure of the project staff is co-terminus with the project.
- SLIET, Longowal does not bear any implications/obligations on the recruited Project staff in a given project.
- Selected candidates will not be permitted to claim any regular/part-time appointments in this institute or any other during this period.
- The Institute reserves the right not to fill up the posts, cancel the advertisement in whole or in part, without assigning any reason and the decision of the Administration of SLIET, Longowal, in this regard shall be final.
- M.E/M.Tech Candidate selected for this position can apply for the regular PhD program in SLIET, Longowal provided they satisfy the eligibility criterion for PhD program in ECE department of SLIET, Longowal.



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**Bio Data Format for Recruitment of Project Associate-I**

**Name** :  
**Gender** :  
**Full Address** :  
**Phone** :  
**Mobile** :  
**E-mail:** :  
**Date of Birth** :  
**Category** :



**Academic Qualifications**

| Sr. No. | Degree | Specialization | University | Year of Passing | % of Marks |
|---------|--------|----------------|------------|-----------------|------------|
|         |        |                |            |                 |            |
|         |        |                |            |                 |            |
|         |        |                |            |                 |            |
|         |        |                |            |                 |            |

**Work experience (if any):**

**Gate/CSIR-UGC-CBSE NET or other National Level Examination:**

**Certificates/scholarships/achievements:**

**Title of MTech. Thesis:**

**Title of Ph.D. Thesis:**

**Publications (Journals) (Give details):**

**List of patents (Give details):**

**Books/book chapters (Give details):**

**Paper Presentations (Give details):**

**Conferences/workshops attended:**

**Skills/Techniques:**

**Expertise in proposed field of research project:**

**Place:**

**Date:**

**Signature of Applicant**